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(54) **Active matrix display device**

(57) This invention is directed to the active matrix display device with an imaging speed rapid enough for the moving image display and the small power consumption. A selector (27) makes the switch between the moving image mode, where the image signal consecutively inputted is consecutively displayed after the certain processing is performed by a data processing unit (21) and the still image mode, where the display is made

based on the image signal stored in a frame memory (25). The messy display upon the switching between the modes can be prevented by differentiating the switching timing of the still to moving image mode from that of the moving to still image mode, improving the display quality.

**EP 1 280 127 A2**

## Description

### BACKGROUND OF THE INVENTION

#### Field of the Invention:

[0001] This invention relates to a display device, which makes a selection between two display modes; a moving image mode where an image signal consecutively inputted is consecutively displayed and a still image mode where an image signal stored in a frame memory is displayed.

#### Description of the Related Art:

[0002] With the spread of personal digital assistant (PDA) in recent years including cellular phone and laptop personal computer, the liquid crystal display (LCD) device and electric luminescence (EL) display device have been used widely as they have relatively small power consumption.

[0003] Fig. 4 shows a circuit diagram of an active matrix LCD as an example of a conventional display device. In the active matrix display device, a controlling circuit 200 is connected to a LCD panel 100.

[0004] The LCD panel 100 comprises a first substrate with a plurality of pixel electrodes and a second substrate with a single common electrode 10 facing to a plurality of the pixel electrodes with a liquid crystal sandwiched between the first and second substrates. On the first substrate, a plurality of the pixel electrodes 1 and a pixel TFT 2 for switching having a thin film transistor (TFT) for each of the pixel electrodes are placed in a matrix configuration. A gate line 3 is placed in the row direction and a data line 4 is placed in the column direction of the matrix of the pixel electrodes 1. The gate line 3 is connected to the gate of the each pixel TFT 2 and the data line 4 is connected to the drain of the each pixel TFT 2. Also, the gate line 3 is connected to a gate line shift resistor 5 placed near the display area. The data line 4 is connected to a data bus line 7 through a data line selection TFT 6, the gate of which is connected to the output terminal of a data line shift resistor 8. The data line selection TFT 6 and the data line shift resistor 8 configure a data line driver for consecutively selecting the data line 4 and supplying the data signal. Also, a storage capacitor 9 for storing a pixel voltage is placed for each of the pixel along with a liquid crystal capacitor placed in parallel.

[0005] The control circuit 200 has a data processing unit 21, a CPU interface 22, a timing controller 23, and a digital-analog converter (DAC) 24. When an analog image signal is inputted, the data processing unit 21 produces a signal suitable for the LCD panel by performing the sampling with an adequate timing, converting the signal into digital signal, adjusting the brightness and contrast, and applying the gamma correction. The CPU interface 22 receives a command of a CPU, not shown

in the figure, which controls a device with a LCD such as PDA and cellular phone, and sends the controlling signal out to each part of the device based on the command received. The timing controller 23 outputs various kinds of timing signal to the LCD panel 100 based on a vertical start signal and a horizontal synchronous signal extracted from the image signal. The DAC 24 converts a RGB digital data outputted from the data processing unit 21 into the voltage suitable for the pixel voltage of the LCD panel 100 and outputs the converted voltage.

[0006] Next, the operation of the active matrix LCD, along with the driver control signal, will be explained. Figs. 5 and 6 are the timing charts showing several timing signals. A vertical synchronous signal Vsync is a clock outputting a "high level" every time when a vertical synchronous period begins for indicating the start of one frame period. A vertical start signal STV is inputted to the gate line shift resistor 5.

The gate line shift resistor 5 is a shift resistor, which starts the operation in response to the vertical start signal STV. A gate line clock CKV is inputted to the gate shift resistor 5 and the shift resistor for each of the gate line clock CKVs consecutively supplies the gate signal to the gate line 3. Half a cycle of the gate line clock CKV is equal to the horizontal synchronous period. Entire pixel TFTs 2 connected to the gate line 3 provided with the gate signal turn on. The horizontal start signal STH is inputted to the data line shift resistor 8 of the data line driver. The data line shift resistor 8 starts the operation in response to the horizontal start signal STH. A data line clock CKH is inputted to the data shift resistor 8 and the output of the data shift resistor 8 changes for each of the data line clock CKHs, consecutively supplying the data line selection signal to the data line selection TFT 6. The data line selection TFT 6 provided with the data line selection signal turns on and the data signal DATA is supplied to the pixel electrode 1 from the data bus line through the data line 4 and the pixel TFT 2. As shown in the figure, there is a plurality of the data bus lines 7. By supplying the same gate signal to the data line selection TFT 6 corresponding to each of the data bus lines, the pixel voltage is simultaneously applied to a plurality of the pixel electrodes 1. After completing the selection of all the data lines 4 by the data shift resistor 8, the gate line clock CKV is inputted again for selecting the next gate line 3. After completing the selection of all the gate lines 3 by the gate shift resistor 5, display of one screen image is completed. Every time data for one row, or, for example, the data for 176 pixels is written, there is a horizontal blanking period, where no data is inputted for a certain period of time. Also, every time the data for entire pixels, or the data for 220 rows, is written, there is a vertical blanking period, where no data is inputted for a certain period of time (for several horizontal period). During the vertical blanking period, the next vertical synchronous signal Vsync is inputted, starting the next frame and repeating the same procedure mentioned above from the beginning.

[0007] In the PDA such as cellular phone, the reduction of the power consumption is indispensable for a longer operation period. Therefore, in cellular phone, a display device with a frame memory capable of storing image data for one screen display is widely used and the display is made by using the data stored in the frame memory. Fig. 7 shows the circuit diagram of the display device with a frame memory. The same components as those in Fig. 4 have the same reference numerals as in Fig. 4 and the explanation about these configurations will be omitted. The frame memory 25 is a SRAM, which stores the digital image data of the entire pixels of the liquid crystal panel 100 inputted through the CPU interface 22. The image data stored in the frame memory 25 is converted into the pixel voltage by the DAC 24 and then supplied to each of the pixel electrodes.

[0008] When the image data stored in the frame memory 25 is displayed, it is necessary to produce the timing signal because the timing signal such as the vertical synchronous signal Vsync is not supplied from outside. An oscillator 26 produces a base clock and supplies it to the timing controller 23. The timing controller 23 produces the data line clock CKH by multiplying the frequency of the basic clock. A counter in the timing controller counts the base clock for outputting one pulse for a predetermined number of data line clocks, producing the horizontal start signal STH and the gate line clock CKV. Also, another counter counts the base clock, producing the vertical start signal STV.

[0009] One of the advantages of the display device with the frame memory 25 is that the power consumption is relatively small since there is no need to input the display data from outside. However, it is necessary to, first, store the image data in the frame memory 25, requiring a certain amount of time for storing. Thus, the device does not have an enough imaging speed for displaying a moving image.

#### SUMMARY OF THE INVENTION

[0010] The object of this invention is directed to a display device with relatively small power consumption capable of displaying a moving image.

[0011] The solution according the invention lies in the features of the independent claims and preferably those of the dependent claims.

[0012] The active matrix display device of this invention has a plurality of gate lines, a plurality of data lines disposed in the direction perpendicular to the gate line, a switching element placed at the crossing of the gate line and the data line, and a plurality of pixel electrodes connected to each of the switching elements. An image signal is supplied to the entire pixel electrodes from the data line for each frame period. And the active matrix display device displays an image based on the pixel voltage between the pixel electrode and the common electrode. The active matrix display device has a moving image mode, where a moving image is displayed based

on the output of the data processing unit which performs a certain processing on consecutively inputted image signal and a still image mode, where a still image is displayed based on the output of the memory which stores the image signal of a plurality of the pixels.

[0013] Also, the switching timing from the still image mode to the moving image mode differs from the switching timing from the moving image mode to the still image mode.

[0014] As to the switching timing from the still image mode to the moving image mode, when a first switching signal, which switches from the still image mode to the moving image mode, is received during one frame period, the still image mode continues until the end of the frame period and the moving image mode begins at the next frame period.

[0015] Likewise, as to the switching timing from the moving image mode to the still image mode, when a second switching signal, which switches from the moving image mode to the still image mode, is received during one frame period, the image signal is read out from the address of the memory corresponding to the pixel supplying the pixel voltage at this moment and the switching to the still image mode is immediately performed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

##### [0016]

Fig. 1 is a circuit diagram of the active matrix liquid crystal display device showing an embodiment of this invention.

Fig. 2 is a timing chart showing a switching timing from a moving image mode to a still image mode of the device of Fig. 1.

Fig. 3 is a timing chart showing the switching timing from the still image mode to the moving image mode of the device of Fig. 1.

Fig. 4 is a circuit diagram of a conventional active matrix liquid crystal display device.

Fig. 5 is a timing chart showing a horizontal blanking period of the device of Fig. 4.

Fig. 6 is a timing chart showing a vertical blanking period of the device of Fig. 4.

Fig. 7 is a circuit diagram of a conventional active matrix liquid crystal display device.

#### DETAILED DESCRIPTION OF THE INVENTION

[0017] Fig. 1 shows a display device of an embodiment of this invention. The same components as those in the device of Figs 4 or 7 are denoted by the same

reference numerals and the explanation about these components will be omitted. A liquid crystal panel 100 of this embodiment is the same as that of the prior arts. In a control circuit 200 of this embodiment, however, a data processing unit 21 and a frame memory 25 are placed. Also, a selector 27, which selects output of the data processing unit 21 or output of the frame memory 25, is provided for switching between a moving image mode and a still image mode. In the moving image mode, the data processing unit 21 produces and outputs a signal suitable for the LCD panel 100 by adjusting the brightness and contrast and applying the gamma correction to the consecutively inputted image signal. And a moving image is displayed based on this signal. In the still image mode, a still image is displayed based on the image signal stored in the frame memory.

**[0018]** In this embodiment, the switching between the moving image mode with a fast imaging speed for displaying a moving image and the still image mode with a slow imaging speed and relatively small power consumption for displaying the still image is made so that the power consumption of the display device can be kept low. In one of use cases of the device, the still image mode is a default use mode. In this case, when a moving image signal is received, or when a user performs a key operation, a CPU, which controls a device with the display device such as cellular phone and PDA, outputs a signal for making the switch from the still image mode to the moving image mode. Then, the CPU outputs a signal for making the switch from the moving image mode to the still image mode when a certain amount of time elapses after a completion of the moving mode, or after the user finishes the key operation. The switching signal is outputted to a CPU interface 22 from the CPU through a timing controller 23, which then performs the switching of the selector 27. The output from the data processing unit 21 and the output from the frame memory 25 is selected, making the switch between the moving image mode and the still image mode.

**[0019]** During the moving image mode, the display operation is performed based on the timing signals shown in Figs. 5 and 6 in the same manner as the conventional devices. In the moving image mode, various kinds of timing signals are external timing signals produced by using a clock extracted from the image signal inputted from outside. And in the still image mode, an internal timing signal produced based on a base clock outputted from an oscillator 26 connected to the timing controller 23 is used. Although these timing signals are basically the same signal, the external timing signal extracted from the external signal and the internal timing signal outputted from the oscillator 26 provided inside the device are differentiated and referred to differently in this specification. For example, among vertical synchronous signals Vsync, the signal extracted from the external signal will be indicated as the external vertical synchronous signal and the signal based on the output from the oscillator will be referred to as the internal ver-

tical synchronous signal.

**[0020]** The display device of this embodiment can be basically operable in the same manner as the device of Figs. 4 and 7. However, the manner for selecting the operation modes is different. Since the external timing signal and the internal timing signal are produced independently from each other, the external vertical synchronous signal and the internal vertical synchronous signal are not totally synchronized. Also, the switching signal for switching between the modes is inputted from the CPU of the device through the CPU interface. And the command for this operation is totally independent from both of the timing signals.

**[0021]** First, a first embodiment relating to the mode switching will be explained. In this embodiment, the switching from the moving image mode to the still image mode will be explained. When a mode-switching signal is inputted, a horizontal counter and a vertical counter of the timing controller are forcibly reset and the display scanning begins from the pixel located at the first row of the first column in the newly selected mode. That is, when the mode-switching signal is inputted, the timing controller 23 outputs a vertical start signal STV and a horizontal start signal STH, starting the operation of a shift resistor. In this case, inside the timing controller 23, there are counters for counting a gate line clock CKV and a data line clock CKH for determining the location of the pixel in terms of row and column provided with the pixel voltage. However, there is a need to reset this counter.

**[0022]** The first embodiment has the following problem. Since the mode-switching signal is not synchronized with the vertical synchronous signal, it is usually inputted during the frame period. However, before this frame period begins, a gate line shift resistor 5 and a data line shift resistor 8 have already started the operation. Suppose the pixel in the n-row of the m-column is provided with the pixel voltage. When the mode-switching signal is inputted under this condition, the counter is forcibly reset, starting the supply of the pixel voltage from the pixel located at the first row of the first column. However, the shift resistor is to select both the pixel at the first row of the first column and the pixel at the n-th row of the m+1th row. As a result, at the frame with the mode-switching is done, the second row and the n+1th row, the third row and the n+2th row are both selected simultaneously, displaying the same images at the upper portion and the lower portion of the screen.

**[0023]** Next, the second embodiment with the better mode-switching scheme will be explained. The switching from the moving image mode to the still image mode will be explained. Fig. 2 is the timing chart for making a switch from the moving image mode to the still image mode. As mentioned above, when an image is displayed in the moving image mode, the operation is based upon the external timing signal inputted from outside. When the image signal is digital, the external timing signal is inputted as the timing signal itself. However, when the

image signal is an analog signal such as a NTSC and a PAL, the external timing signal is extracted from the image signal. In some cases, the signal is extracted inside of the control circuit 200, it will be, however, referred to as the external timing signal here. Suppose the switching signal for making the switch from the moving image mode to the still image mode (it will be indicated as the moving to still image switching signal) is received. The vertical counter inside of the timing controller is reset by the vertical start signal STV for counting the gate line clock CKV and the horizontal counter is reset by the horizontal start signal STH for counting the data line clock CKH, resulting in the counting value of (n, m) of these counters. Therefore, this counting value is showing the coordinates of the pixel provided with the pixel voltage at this moment. If the image signal is read out from the address of the frame memory 25 corresponding to this counting value, the image signal corresponding to the next pixel electrode can be read out from the frame memory 25. When the moving to still image switching signal is inputted to the timing controller 23 through the CPU interface 22, the internal timing signal can be outputted without resetting the counting value of the vertical counter or the horizontal counter. Then the selector 27 is switched for selecting the frame memory 25, and the switching to the still image mode is immediately made. The image signal is supplied to the next pixel electrode from the corresponding address of the frame memory 25. In this way, two gate lines are not selected at the same time. Thus, there is no messy display upon the switching between the modes.

**[0024]** Although the data clock (the base clock) of the external timing signal and the base clock outputted from the oscillator 26 are not synchronized, it does not cause any problem because the counter inside of the timing controller is not reset. The operation stops just a short period of time, about one cycle of the base clock upon the switching between the modes. In this embodiment, the timing controller 23 is set up not to output the clock shorter than one base clock for preventing the false operation. Therefore, upon the switching between the modes, the operation stops for more than one cycle of the base clock, about the  $\Delta t$  period shown in the figure,.

**[0025]** Next, the switching from the still image mode to the moving image mode will be explained. Fig. 3 is a timing chart of the switching from the still image mode to the moving image mode. When the switching signal for making the switch from the still image mode to the moving image mode (it will be indicated as the still to moving image switching signal) is received, the switching of the operation is not particularly performed. The operation by the internal timing signal based on the output of the oscillator 26, that is, the still image mode continues till the end of the frame memory. The next internal vertical synchronous signal is not outputted. Then, after the  $\Delta t_2$  period passes, the external vertical synchronous signal is inputted. Therefore, at the beginning of the frame period after the external vertical synchronous sig-

nal is inputted, the mode is switched to the moving image mode based on the external timing signal. In this way of switching, two gate lines are not selected at the same time. Thus, there is no messy display upon the switching between the modes.

**[0026]** During the  $\Delta t_2$  period between the still image mode and the moving image mode, there is no need to supply the clock. However, since it is difficult to stably supply the various external timing signals simultaneously with the input of the external vertical synchronous signal, the external timing signal should be outputted several base clocks prior to the input of the external vertical synchronous signal. During the  $\Delta t_2$  period, although the timing signal is supplied, the shift resistors 5, 8 do not start the operation because the vertical start signal STV or the horizontal start signal STH are not supplied. It is also possible to switch to the external timing signal immediately after the frame period of the still image mode.

**[0027]** In the still image mode, the image signal and the timing signal are supplied within the control circuit 200. But in the moving image mode, the image signal is supplied from outside and the still image is displayed in the synchronization with the external signal. Therefore, in the second embodiment, the switching timing from the still image mode to the moving image mode and the switching timing from the moving image mode to the still image mode are different from each other. Each switching is performed through the most preferable procedure, improving the display quality.

**[0028]** In the embodiments described above, the liquid crystal display device is explained as an example of the active matrix display device. However, this invention is not limited to these embodiments. It is also applicable to EL display device, LED display device and vacuum luminescence display device.

**[0029]** The display device of this invention makes the display by making the switch between two modes; the moving image mode with the rapid imaging speed where the image is displayed based on the output from the data processing unit 21, and the still image mode with small power consumption where the image is displayed based on the output of the memory 25. Therefore, the display device with the small power consumption and yet with the high quality display is achieved.

**[0030]** Furthermore, the switching timing from the still image mode to the moving image mode and the switching timing from the moving image mode to the still image mode are different from each other. Each switching is performed through the most preferable procedure, improving the display quality.

**[0031]** In the active matrix display device having the data processing unit 21 consecutively outputting the image signal after performing a certain processing to the image signal consecutively inputted, the memory element 25 holding the image signal for a plurality of pixels, and the switching device selecting the data processing unit or the memory element, the configuration of the display panel 100 can be exactly the same as that of the

conventional devices. Only the configuration of the control circuit 200 should be modified, suppressing the manufacturing cost.

[0032] When the still to moving image switching signal is received during the frame period in the still image mode, the still image mode continues till the end of this particular frame period and the next internal vertical synchronous signal is not produced. Then, after this frame period, when the next external vertical synchronous signal is inputted, the display in the moving image mode starts. Therefore, the device of this invention can be embodied with a relatively simple configuration.

[0033] Also, since it is possible to read out the image signal from the address of the memory corresponding to the counting value of the vertical counter and the horizontal counter when the moving to still image switching signal is received, the device of this invention can be embodied with a relatively simple configuration.

### Claims

#### 1. An active matrix display device comprising:

a plurality of gate lines (3) disposed in a direction;

a plurality of data lines (4) disposed in a direction different from the direction of the gate lines (3);

a plurality of switching elements (2) each disposed at corresponding intersections of the gate lines (3) and the data lines (4);

a plurality of pixel electrodes (1) each connected to the corresponding switching elements (2), an image signal being supplied to the entire pixel electrodes (1) from the data lines (4) during a frame period,

a plurality of pixels each having the corresponding pixels electrodes (1);

a data processing unit (21) receiving, processing and outputting the image signal for displaying a moving image in a moving image mode; and

a memory (25) holding the image signal for displaying a still image in a still image mode.

2. The active matrix display device of claim 1, further comprising a switching device (27) selecting the data processing unit (21) in the moving image mode or the memory (25) in the still image mode.

3. The active matrix display device of claims 1 or 2,

wherein a switching timing from the still image mode to the moving image mode and a switching timing from the moving image mode to the still image mode are different.

4. The active matrix display device according to any of claims 1 to 3, wherein the still image mode continues until an end of the frame period when a first switching signal for switching from the still image mode to the moving image mode is received during the frame period and the moving image mode starts from a next frame period.

5. The active matrix display device of claim 1, wherein the image signal is read out from an address of the memory (25) corresponding to one of the pixels provided with a pixel voltage and the still image mode starts immediately when a second switching signal for switching from the moving image mode to the still image mode is received during the frame period.

6. The active matrix display device of claim 4, wherein the display device operates based on an external vertical synchronous signal which is a timing signal outputted at a beginning of the frame period as a pulse and synchronized with the image signal inputted from outside in the moving image mode and the display device produces an internal vertical synchronous signal inside the device in the still image mode, the still image mode continues until the end of the frame period without producing a next internal vertical synchronous signal when the switching signal is received during the frame period in the still image mode, and the moving image mode begins when the frame period is completed and the display device receives the external vertical synchronous signal.

7. The active matrix display device of claim 4, wherein a switching timing from the still image mode to the moving image mode and a switching timing from the moving image mode to the still image mode are different.

8. An active matrix display device comprising:

a plurality of gate lines (3) disposed in a direction, each of the gate lines (3) being consecutively selected based on a gate line clock;

a plurality of data lines (4) disposed in a direction different from the direction of the gate lines (3), each of the data lines being consecutively selected based on a data line clock;

a plurality of switching elements (2) each dis-

posed at corresponding intersections of the gate lines (3) and the data lines (4);

a plurality of pixel electrodes (1) each connected to the corresponding switching elements (2), an image signal being supplied to the entire pixel electrodes (1) from the data lines during a frame period,

a plurality of pixels each having the corresponding pixels electrodes (1); and

a memory (25) holding the image signal for displaying a still image in a still image mode,

wherein the still image mode starts immediately when a switching signal for switching from a moving image mode to the still image mode is received during the frame period by reading out the image signal from an address of the memory corresponding to the pixel provided with a pixel voltage.

9. The active matrix display device of claim 8, further comprising a vertical counter counting the gate line clock, a horizontal counter counting the data line clock, or a combination of the vertical counter and the horizontal counter, wherein the image signal is read out from the address of the memory (25) based on a counted value of the vertical counter, a counted value of the horizontal counter, or counted values of the vertical and horizontal counters when the switching signal for switching from the moving image mode to the still image mode is received.
10. The active matrix display device of claim 8, wherein a switching timing from the still image mode to the moving image mode and a switching timing from the moving image mode to the still image mode are different.
11. A control device of an active matrix display device displaying a moving image or a still image in a frame period, the display device including pixels having corresponding pixel electrodes (1), an image signal being supplied to the entire pixel electrodes (1), the control device comprising;  
a data processing unit (21) receiving, processing and outputting the image signal for displaying the moving image;  
a memory (25) holding the image signal for displaying the still image; and  
a switching device (27) selecting the data processing unit (21) or the memory (25).
12. The control device of an active matrix display device of claim 11, wherein a switching timing from the data processing unit to the memory (25) and a switching timing from the memory to the data processing unit

(21) are different.

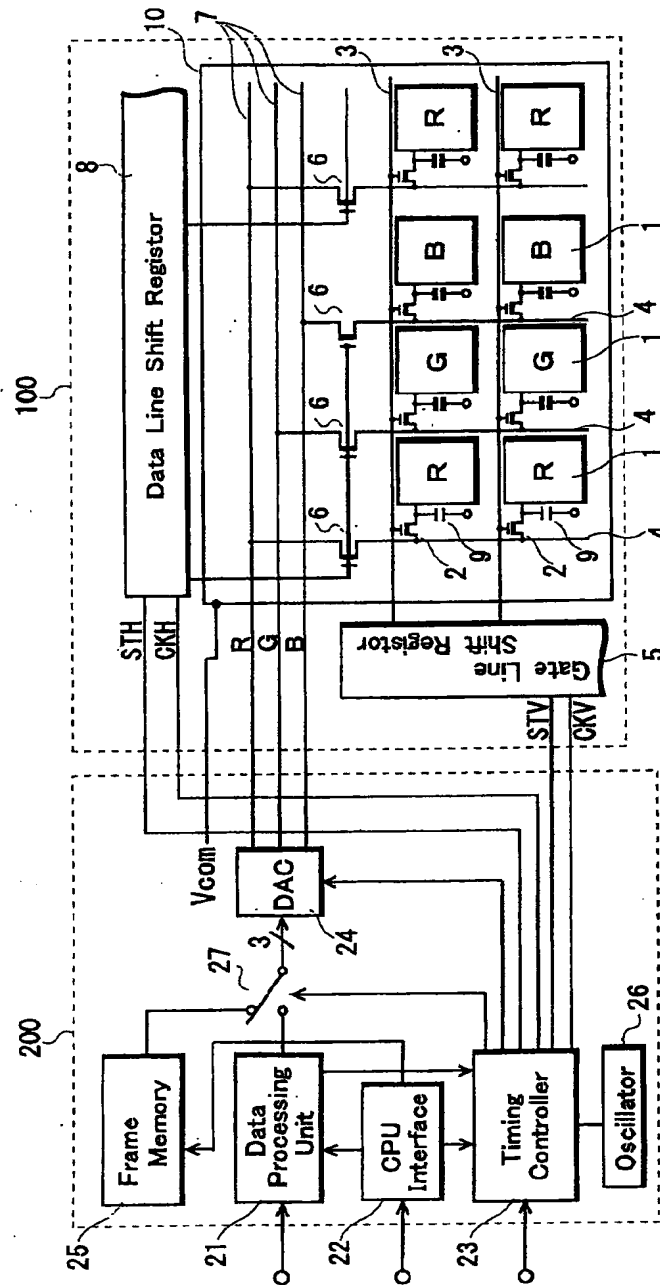
13. The control device of an active matrix display device of claim 11, wherein the memory (25) is selected until an end of the frame period when a first switching signal for switching from the memory (25) to the data processing unit is received during the frame period and the data processing unit is selected from a next frame period.
14. The control device of an active matrix display device of claim 11, wherein the image signal is read out from an address of the memory (25) corresponding to one of the pixels provided with a pixel voltage and the memory (25) is selected immediately when a second switching signal for switching from the data processing unit to the memory (25) is received during the frame period.
15. The control device of an active matrix display device of claim 13, further comprising a timing controller (23) outputting internal timing signals including an internal vertical synchronous signal outputted as a pulse for the frame period.
16. The control device of an active matrix display device of claim 15, further comprising an oscillator (26) connected to the timing controller (23), wherein the device operates based on external timing signals including an external synchronous signal outputted at a beginning of the frame period and synchronizes with the image signal inputted from outside while the data processing unit is selected, the display device operates based on the internal vertical synchronous signal produced by the timing controller (23) according to an output from the oscillator (26) while the memory (25) is selected, and the timing controller (23) continues to produce the internal timing signals but does not produce a next internal vertical synchronous signal when the first switching signal is received while the memory (25) is selected, and the operation of the display device based on the external timing signals resumes after the frame period ends when a next external vertical synchronous signal is inputted.
17. The control device of an active matrix display device claim 15, wherein a switching timing from the data processing unit to the memory (25) and a switching timing from the memory (25) to the data processing unit are different.
18. A control device of an active matrix display device displaying a moving image or a still image in a frame period, the display device including pixels having corresponding pixel electrodes (1), a plurality of gate lines (3) and a plurality of data lines (4), an im-

age signal being supplied to the entire pixel electrodes (1), the control device comprising;  
 a data processing unit (21) receiving, processing and outputting the image signal for displaying the moving image;  
 a memory (25) holding the image signal for displaying the still image;  
 a switching device (27) selecting the data processing unit (21) or the memory (25); and  
 a timing controller (23) outputting internal timing signals including an internal vertical synchronous signal outputted as a pulse for the frame period, a gate line clock for selecting one of the gate lines (3) and a data line clock for selecting one of the data lines (4),  
 wherein the image signal is read out from an address of the memory (25) corresponding to the gate line (3) and the data line (4) which are selected when a switching signal for switching from the data processing unit (21) to the memory (25) is received, and the memory (25) is selected immediately when the switching signal is received.

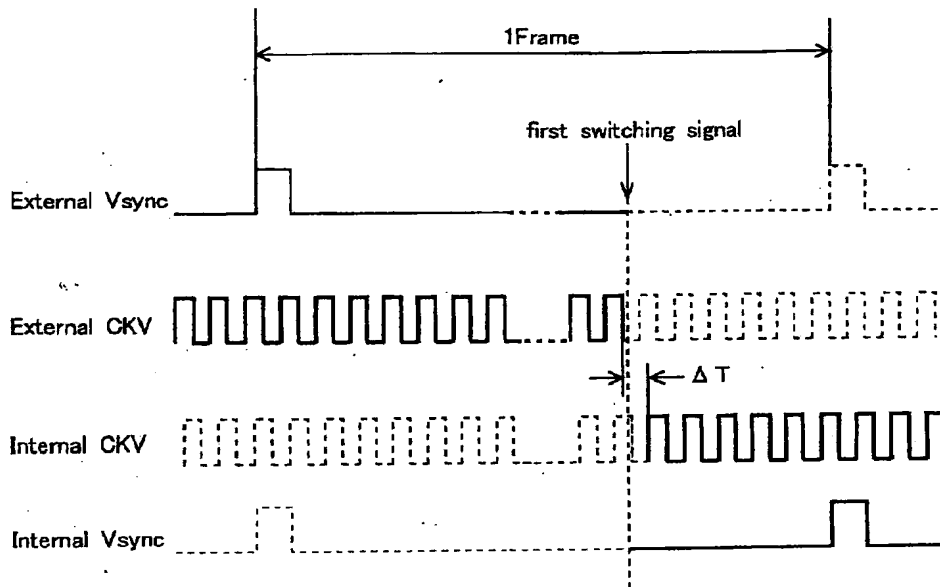
19. The control device of an active matrix display device of claim 18, further comprising a vertical counter counting the gate line clock, a horizontal counter counting the data line clock, or a combination of the vertical counter and the horizontal counter, wherein the image signal is read out from the address of the memory (25) based on a counted value of the vertical counter, a counted value of the horizontal counter, or counted values of the vertical and horizontal counters when the switching signal is received.
20. The control device of an active matrix display device of claim 18, wherein a switching timing from the memory (25) to the data processing unit (21) and the switching timing from the data processing unit (21) to the memory (25) are different.



Fig.1



**Fig.2**



**Fig.3**

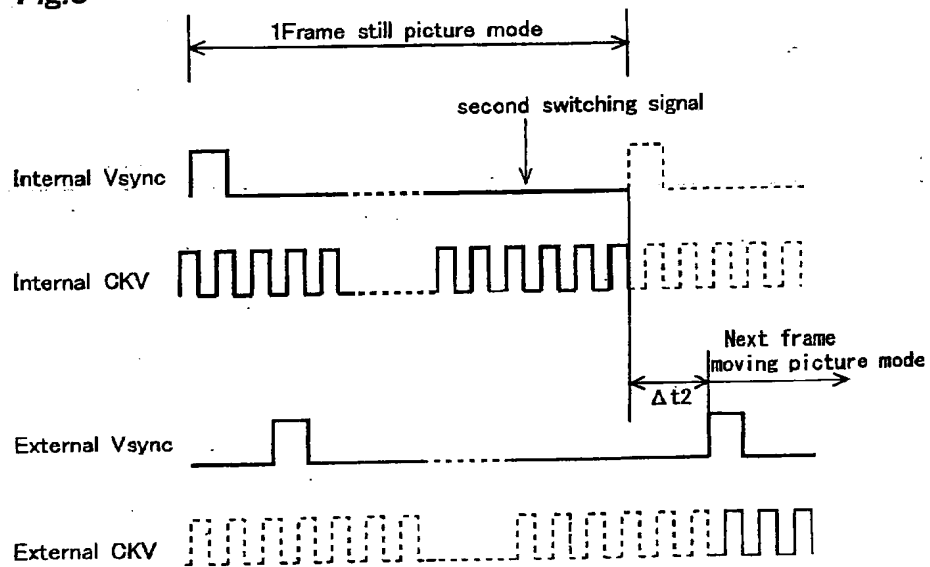


Fig.4

PRIOR ART

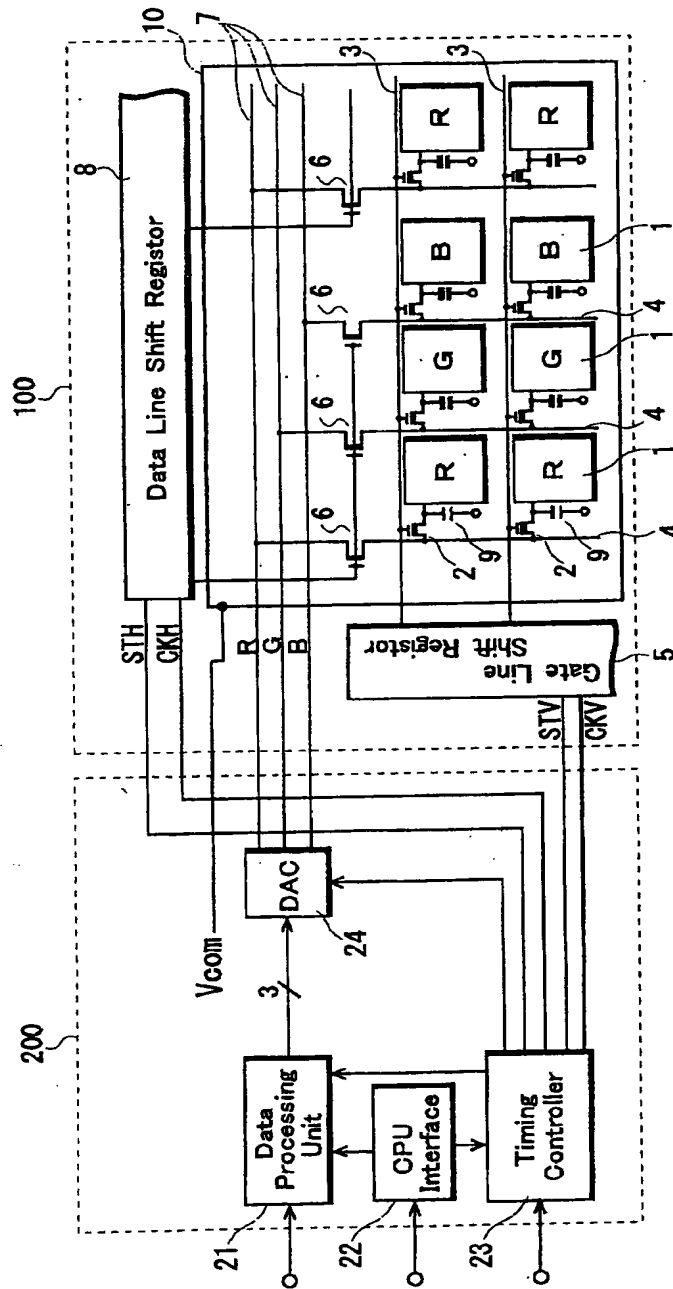


Fig.5

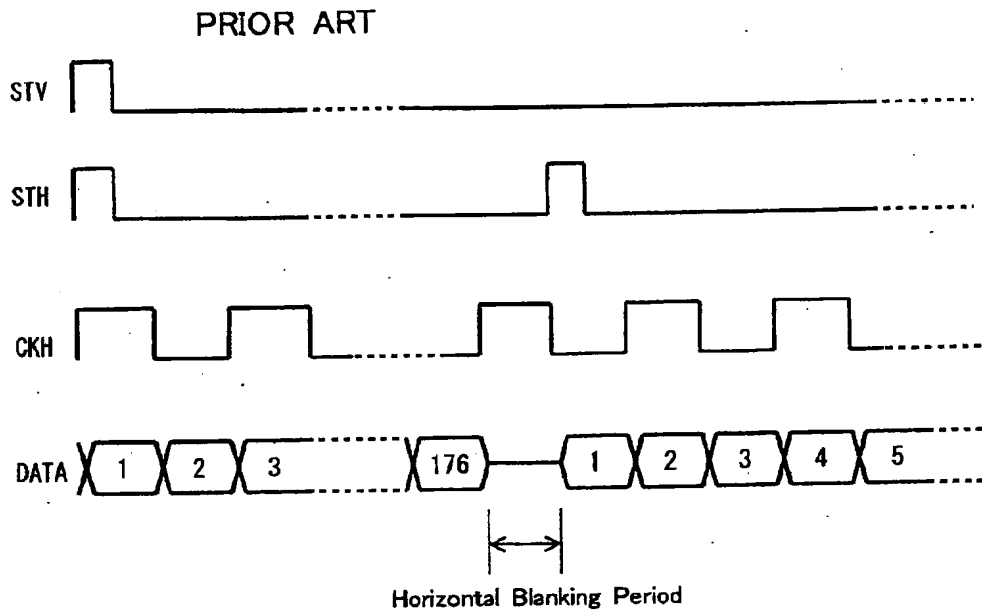


Fig.6

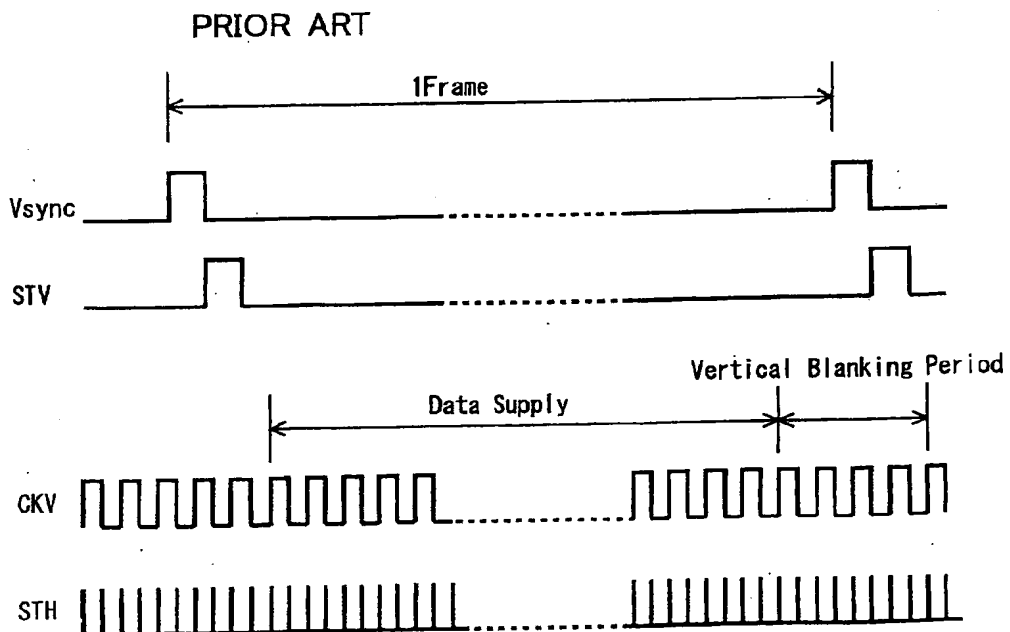


Fig.7

PRIOR ART

